


ACEII SCHEMATICS

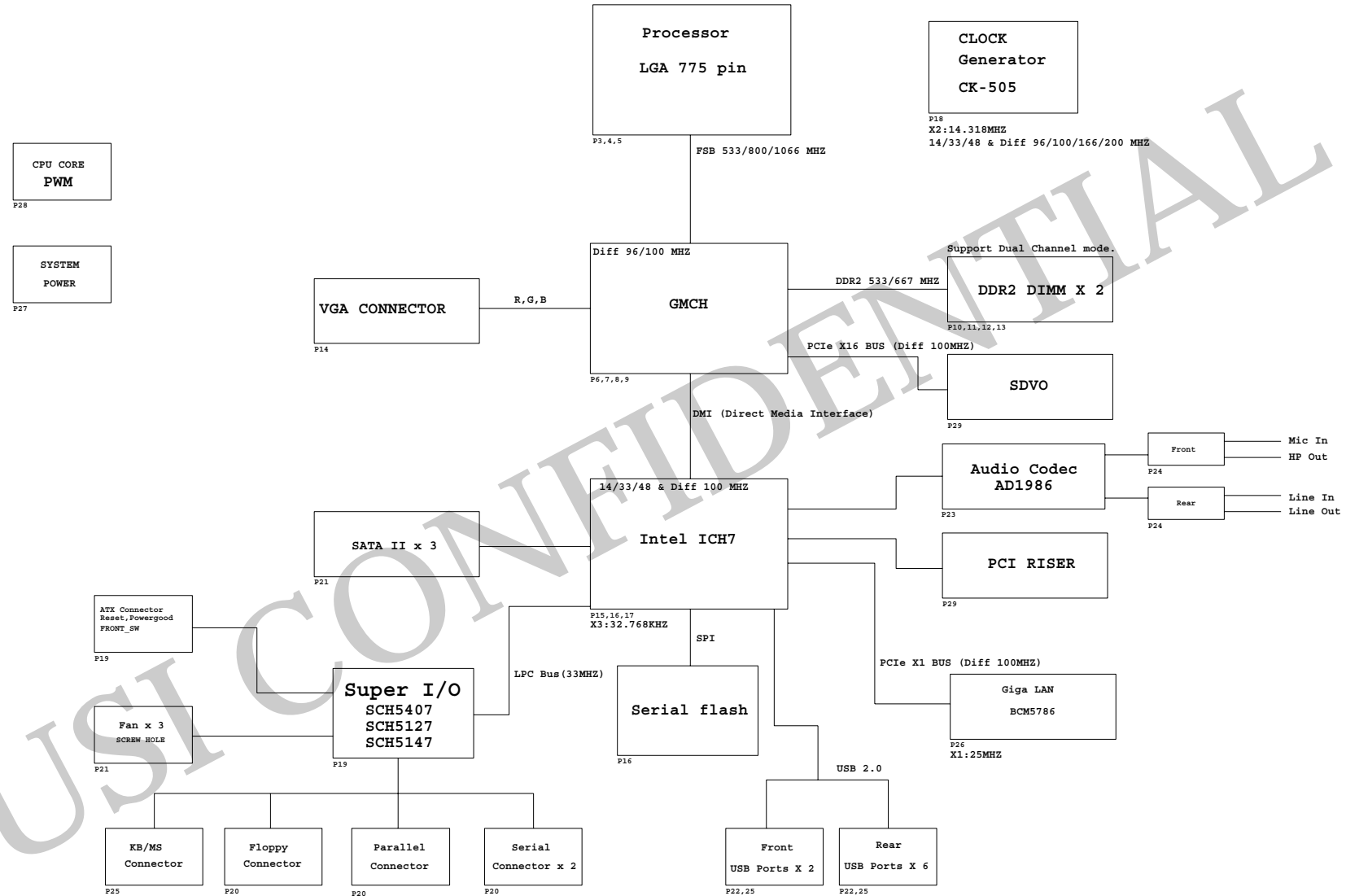
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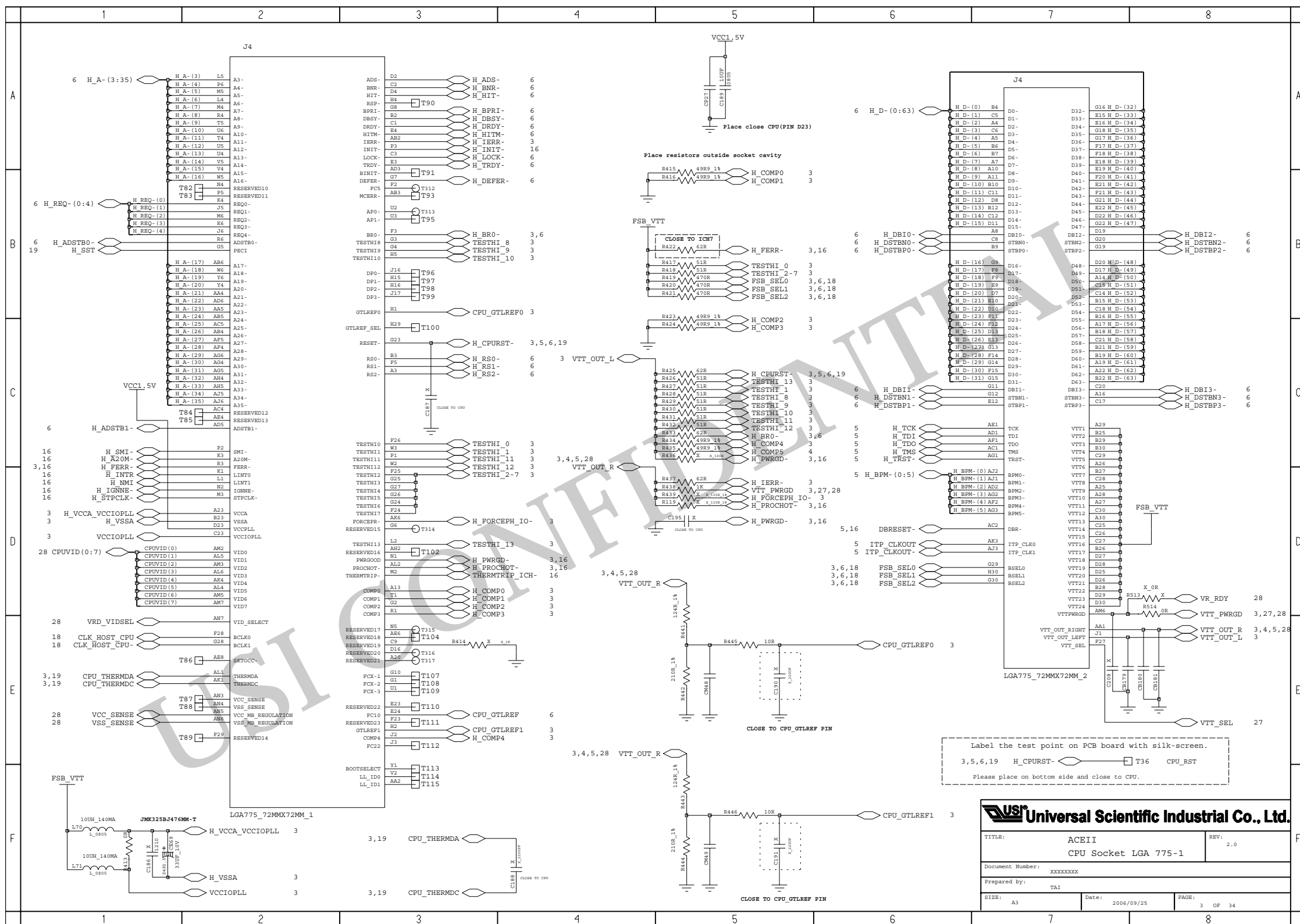
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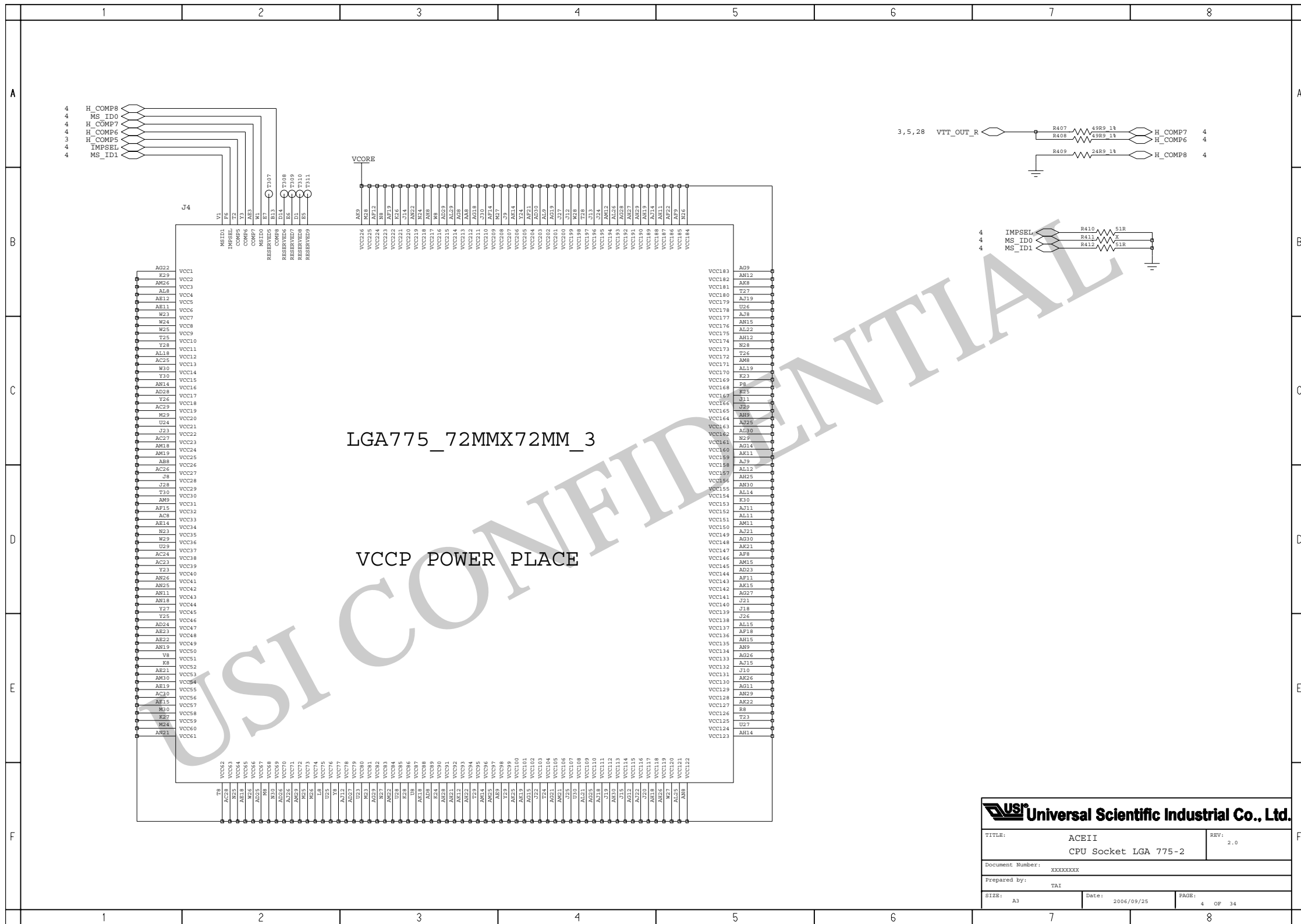
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ACEII BLOCK DIAGRAM





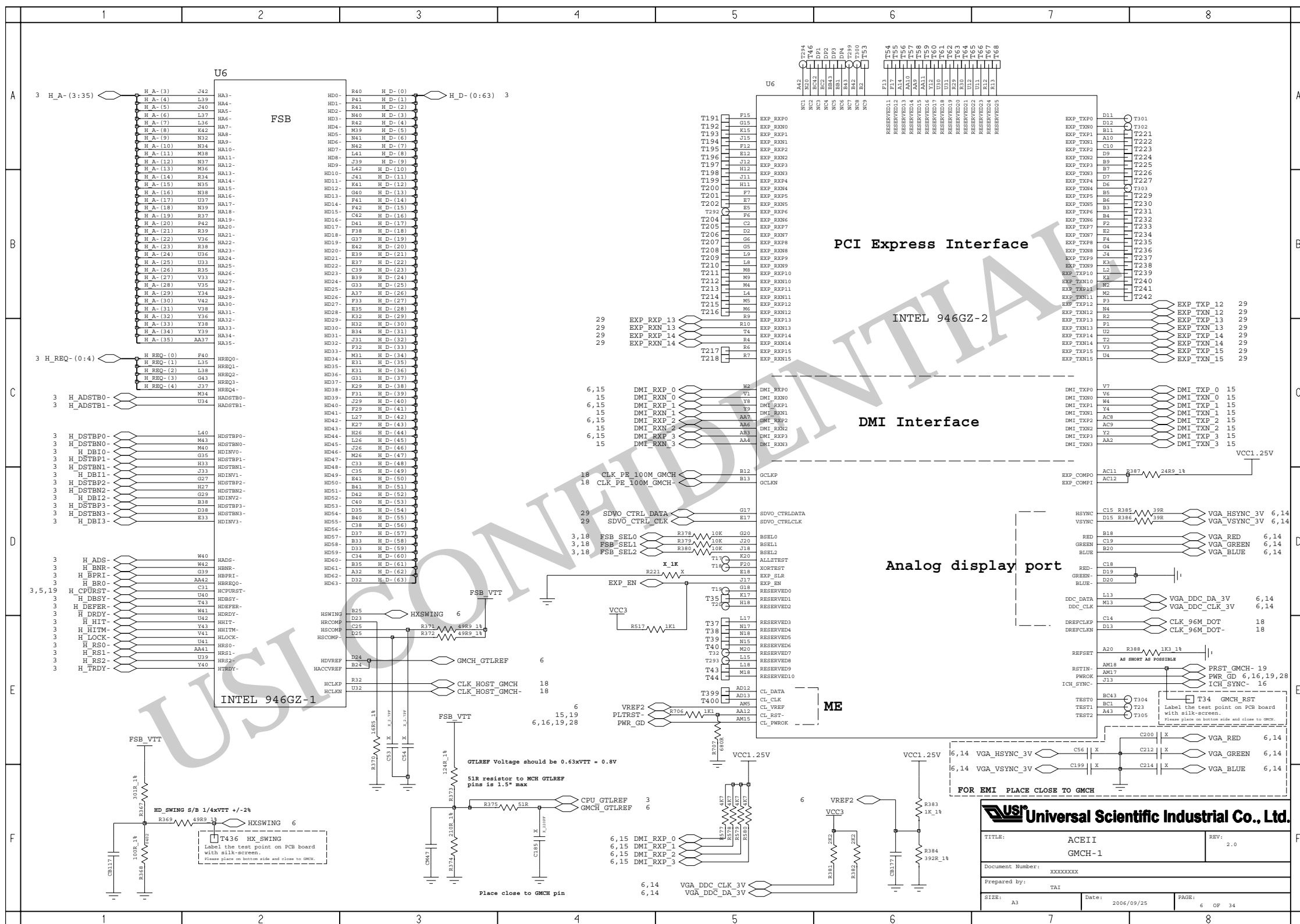


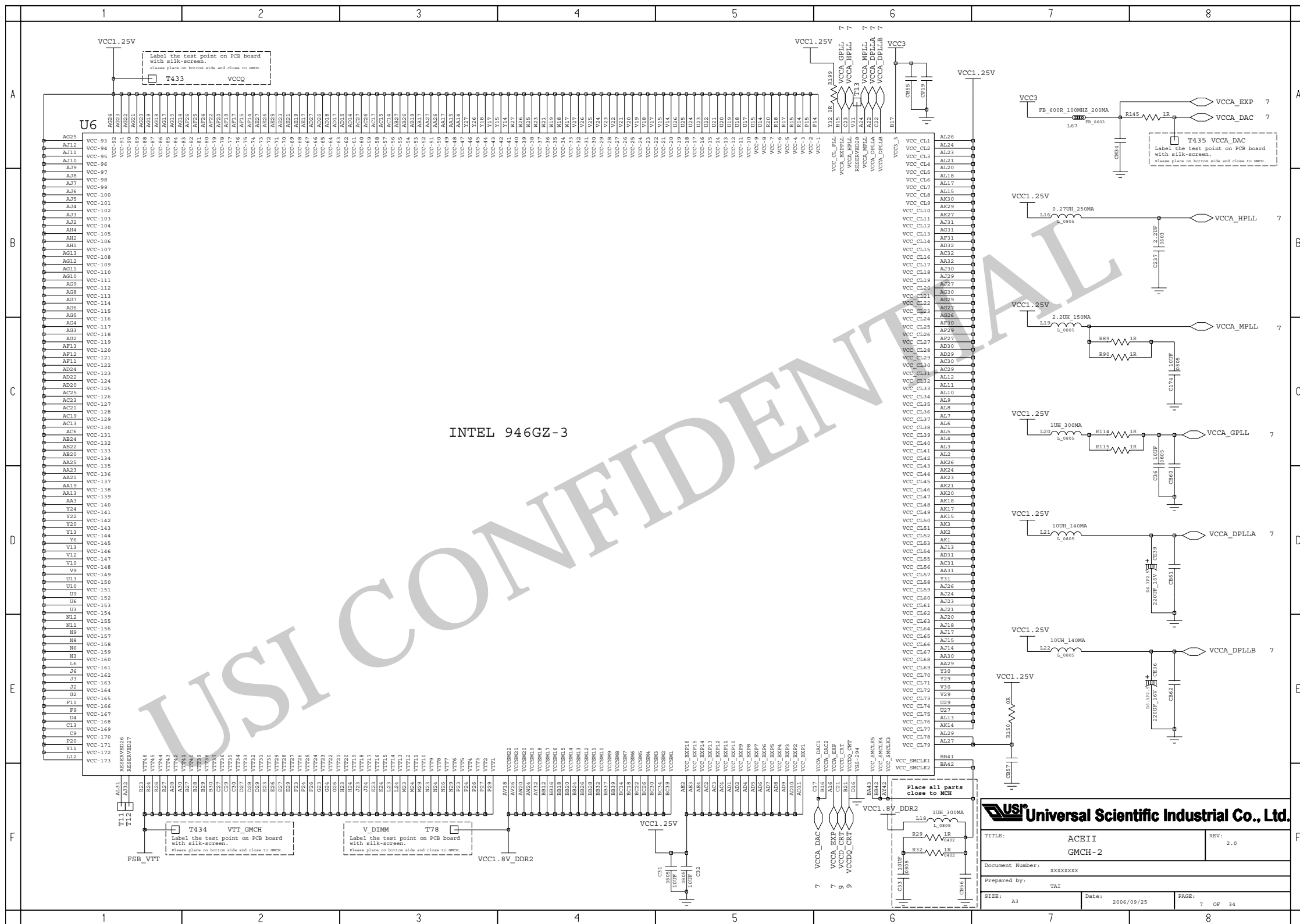
LGA775_72MMX72MM_4

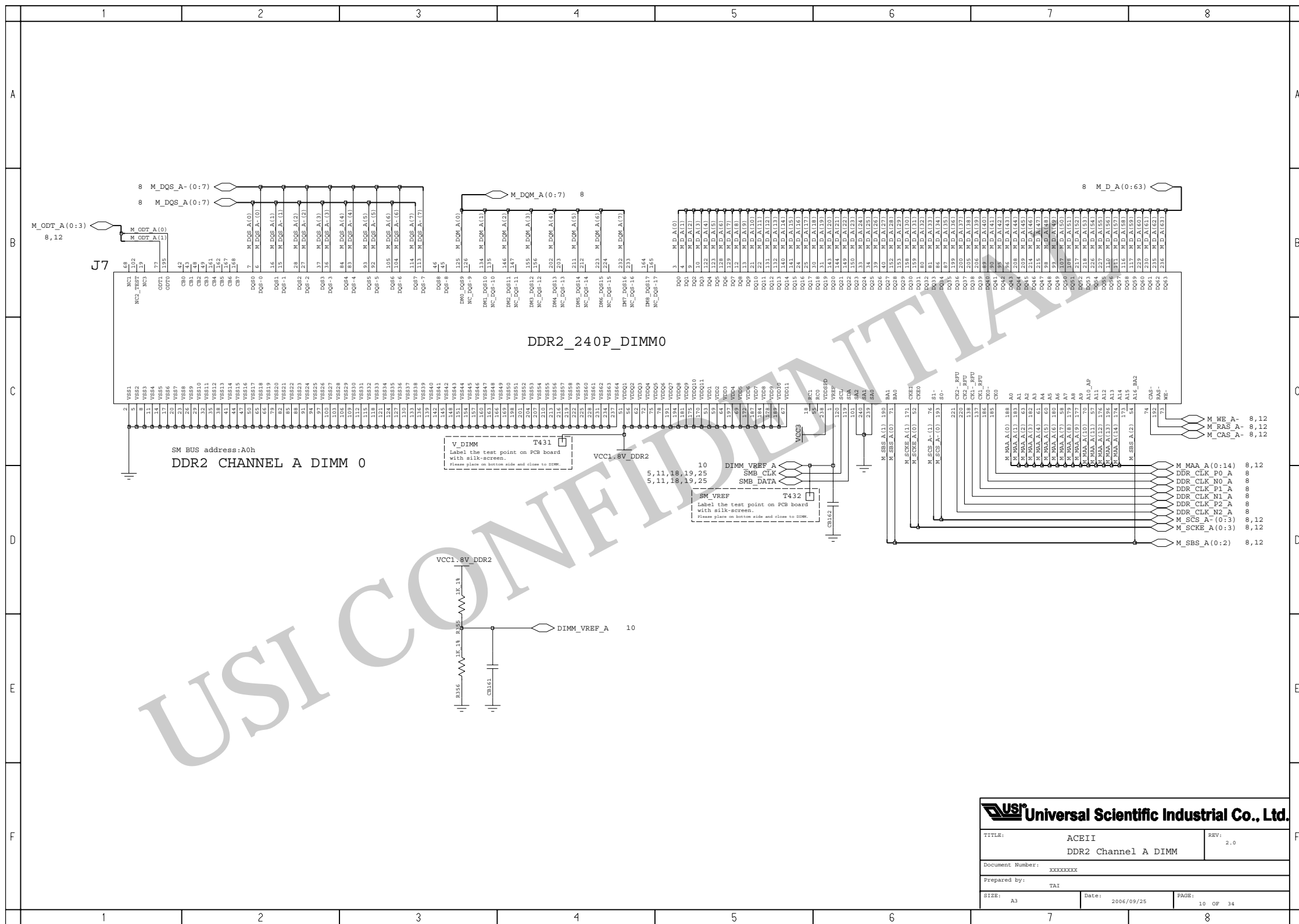
VSS GROUND PLACE

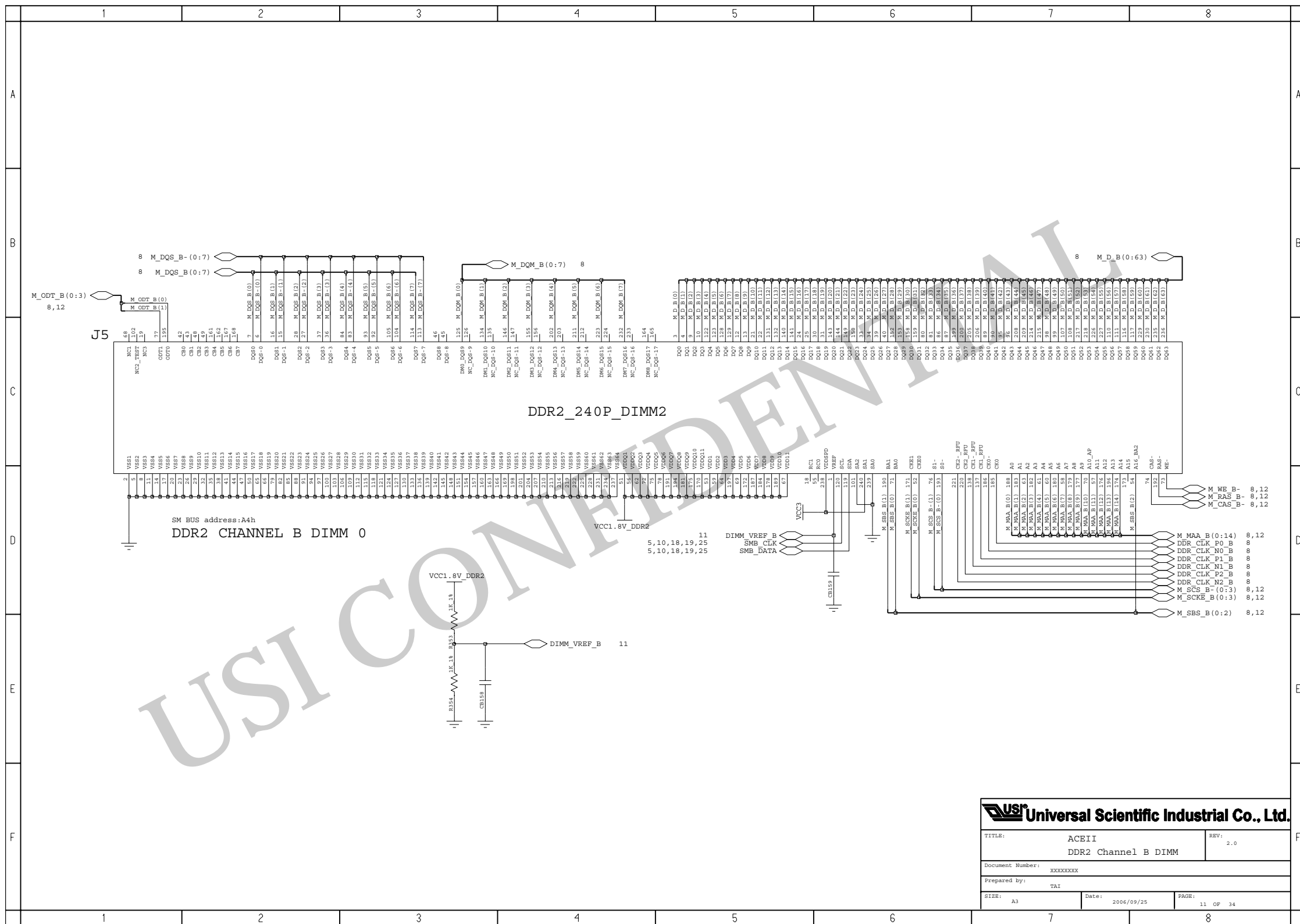
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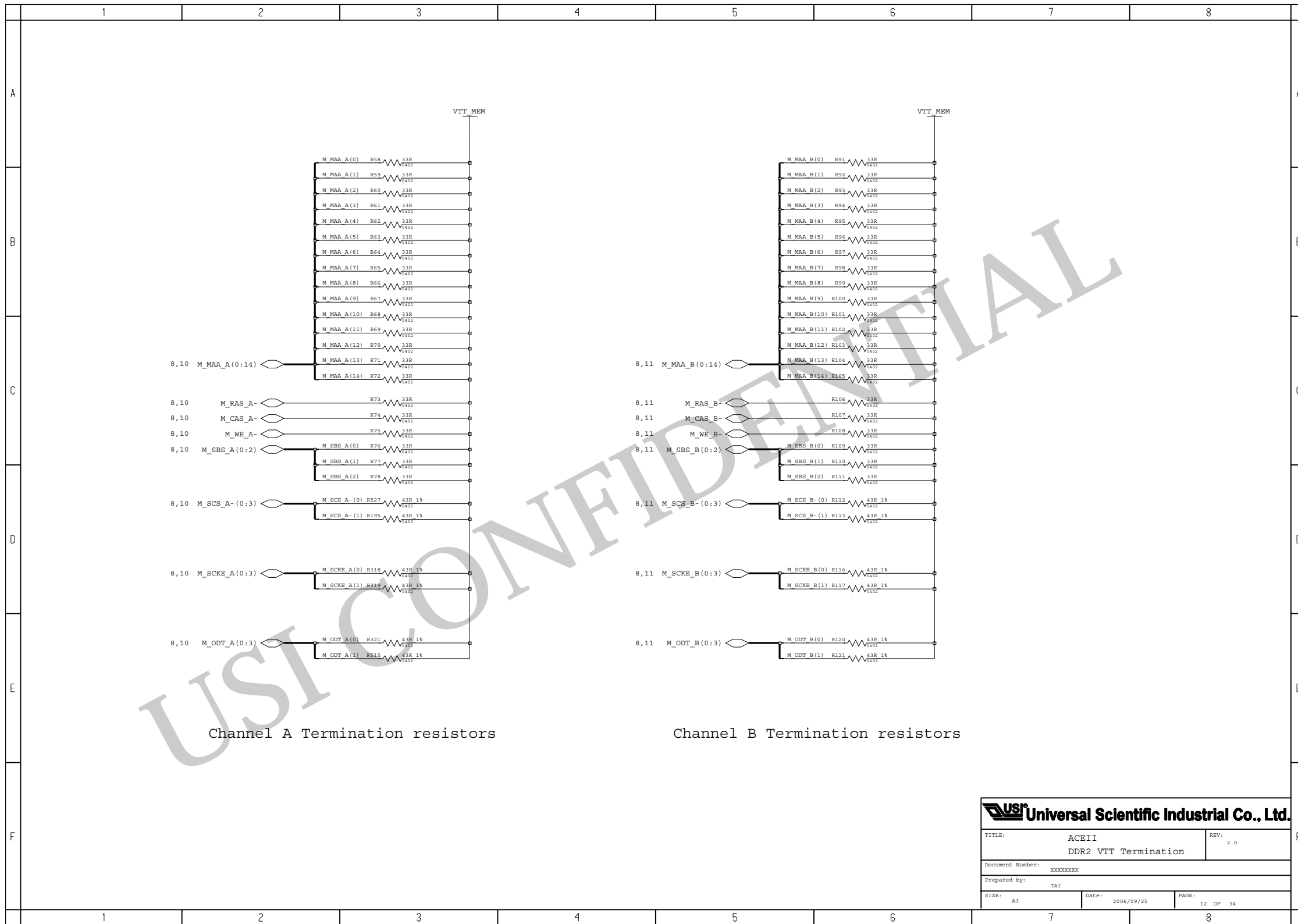
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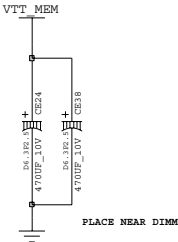
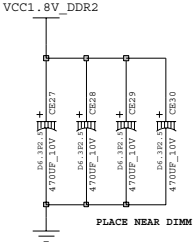
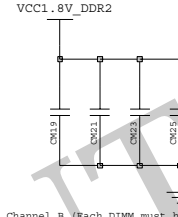
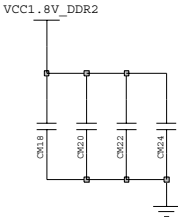
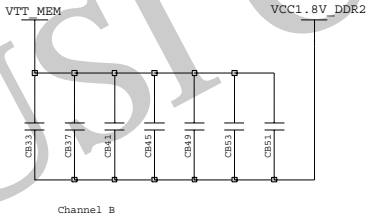
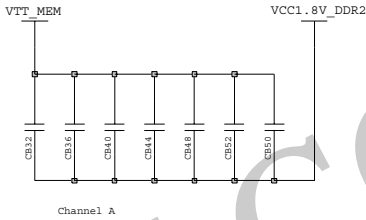
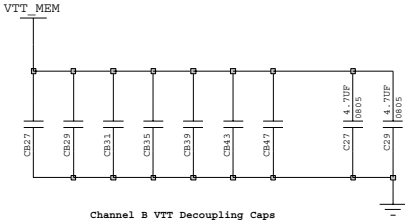
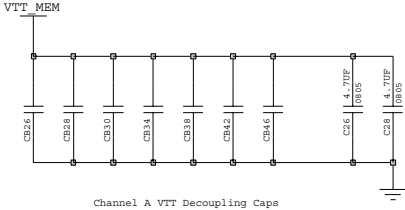


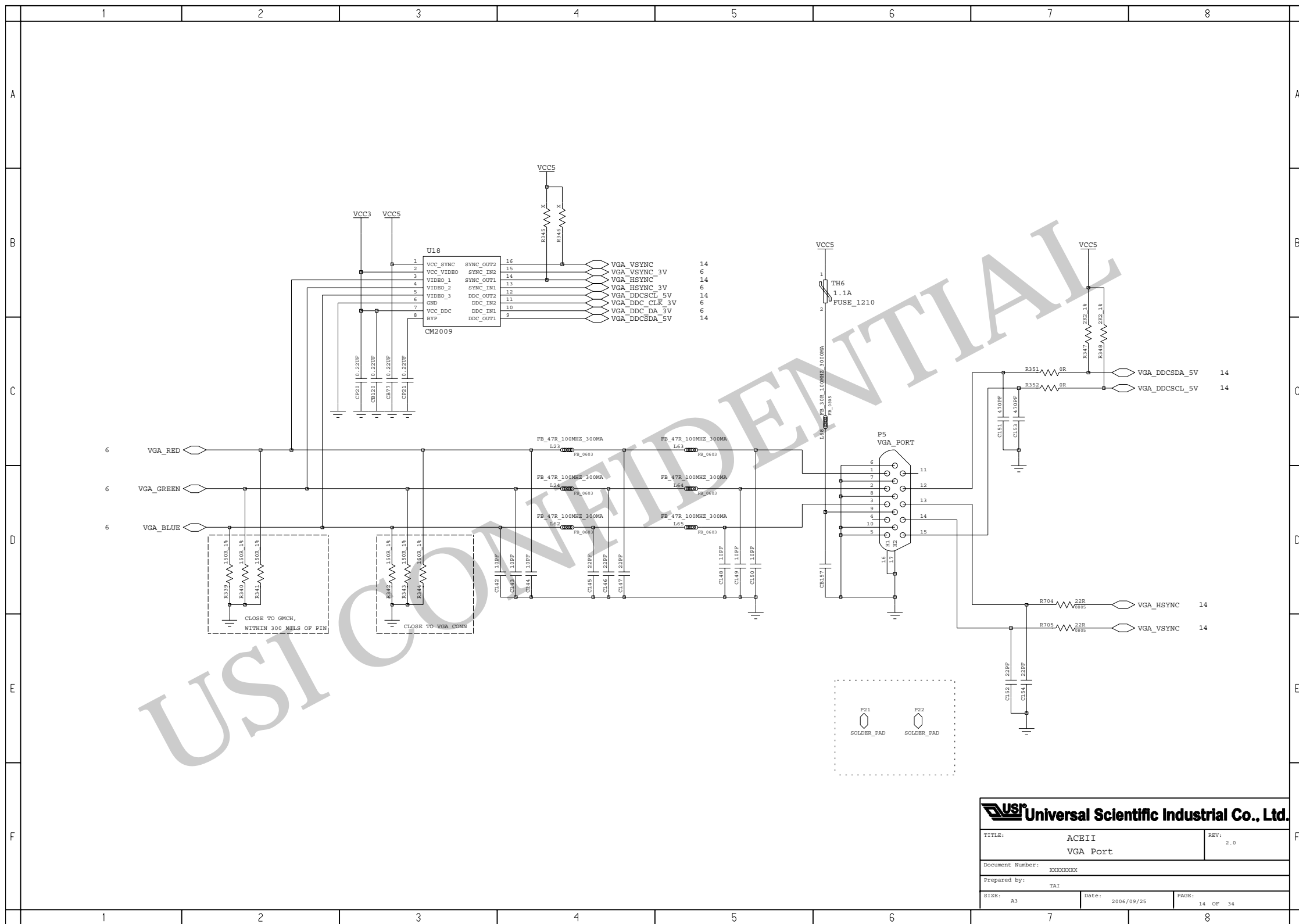


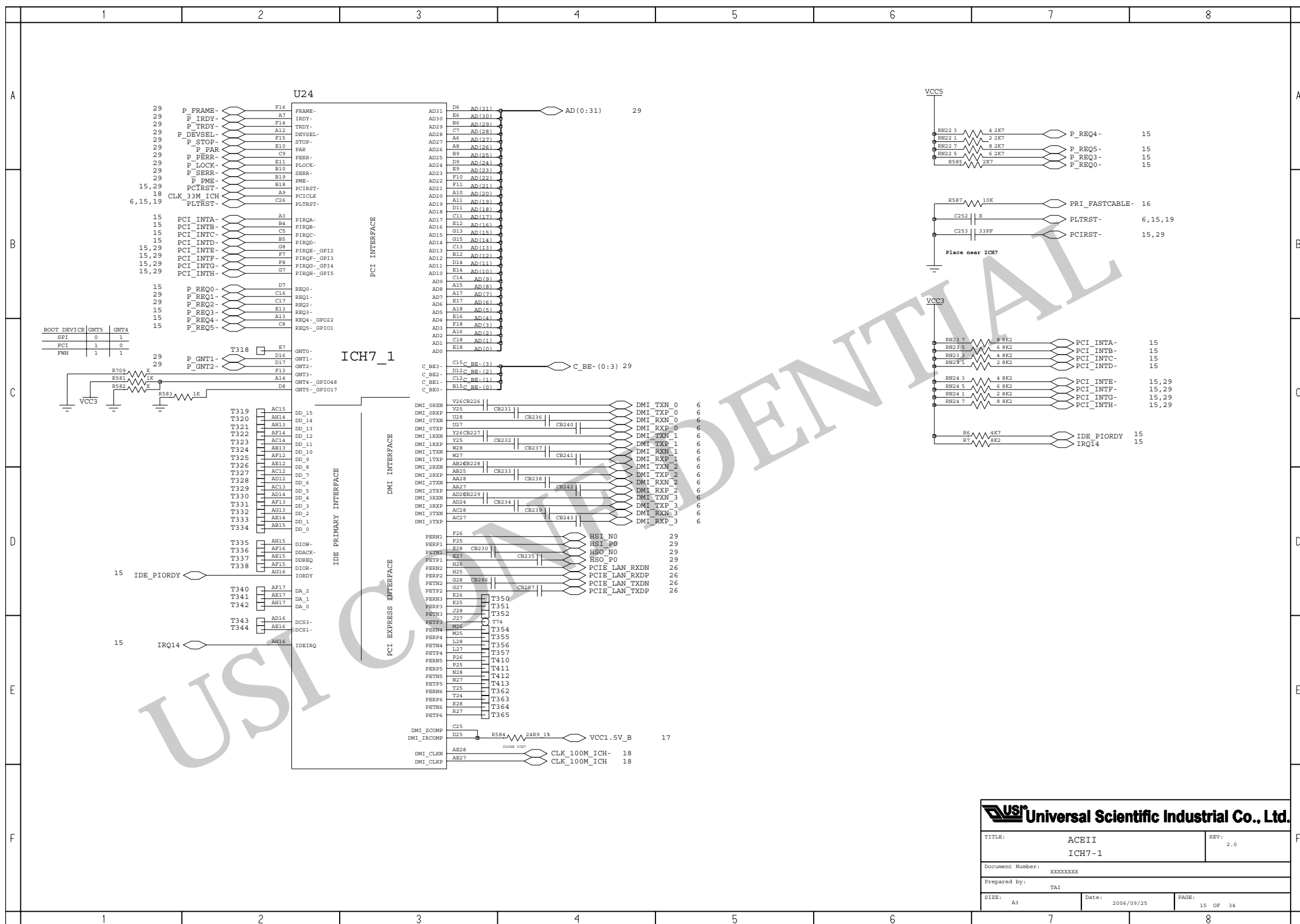


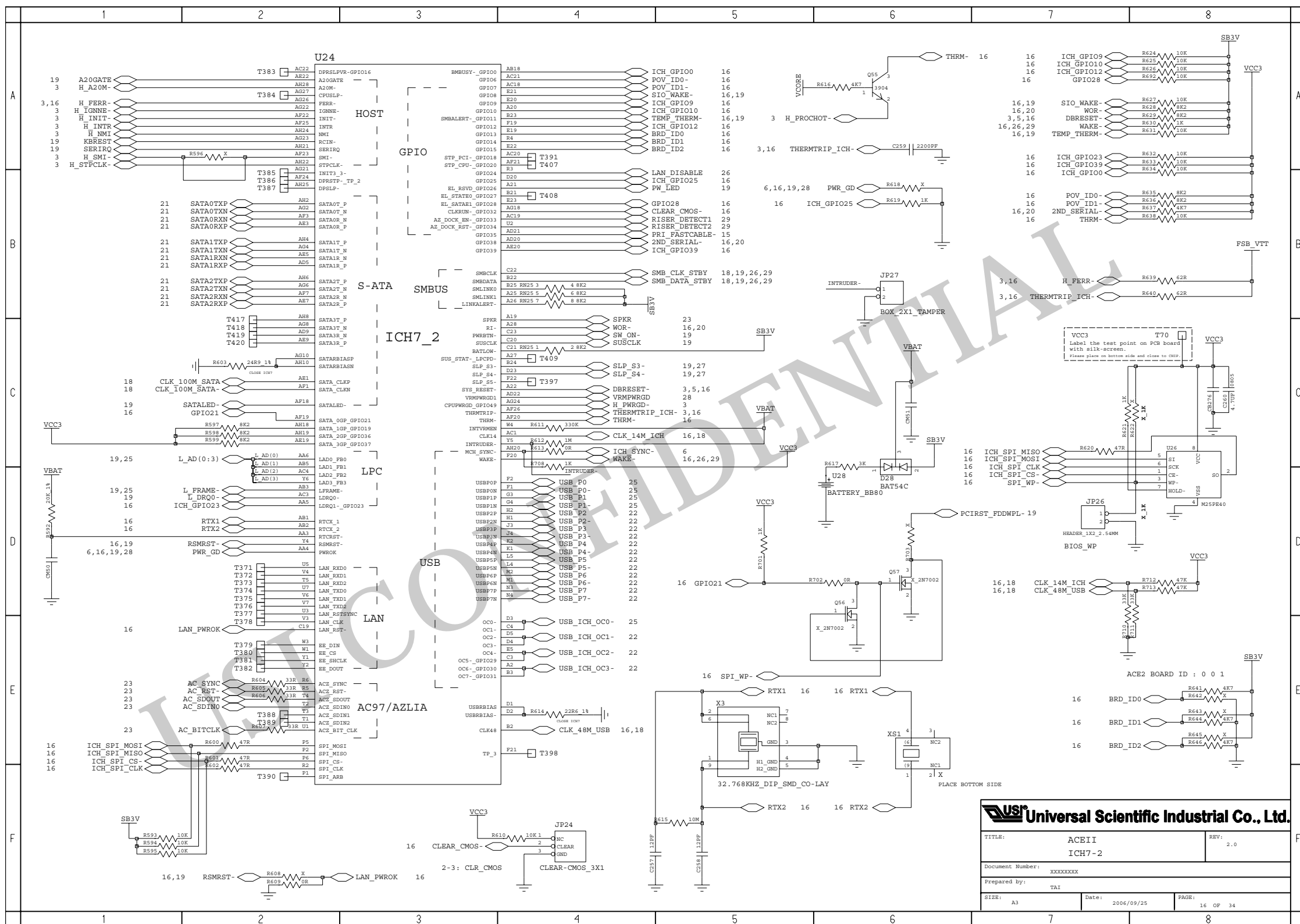


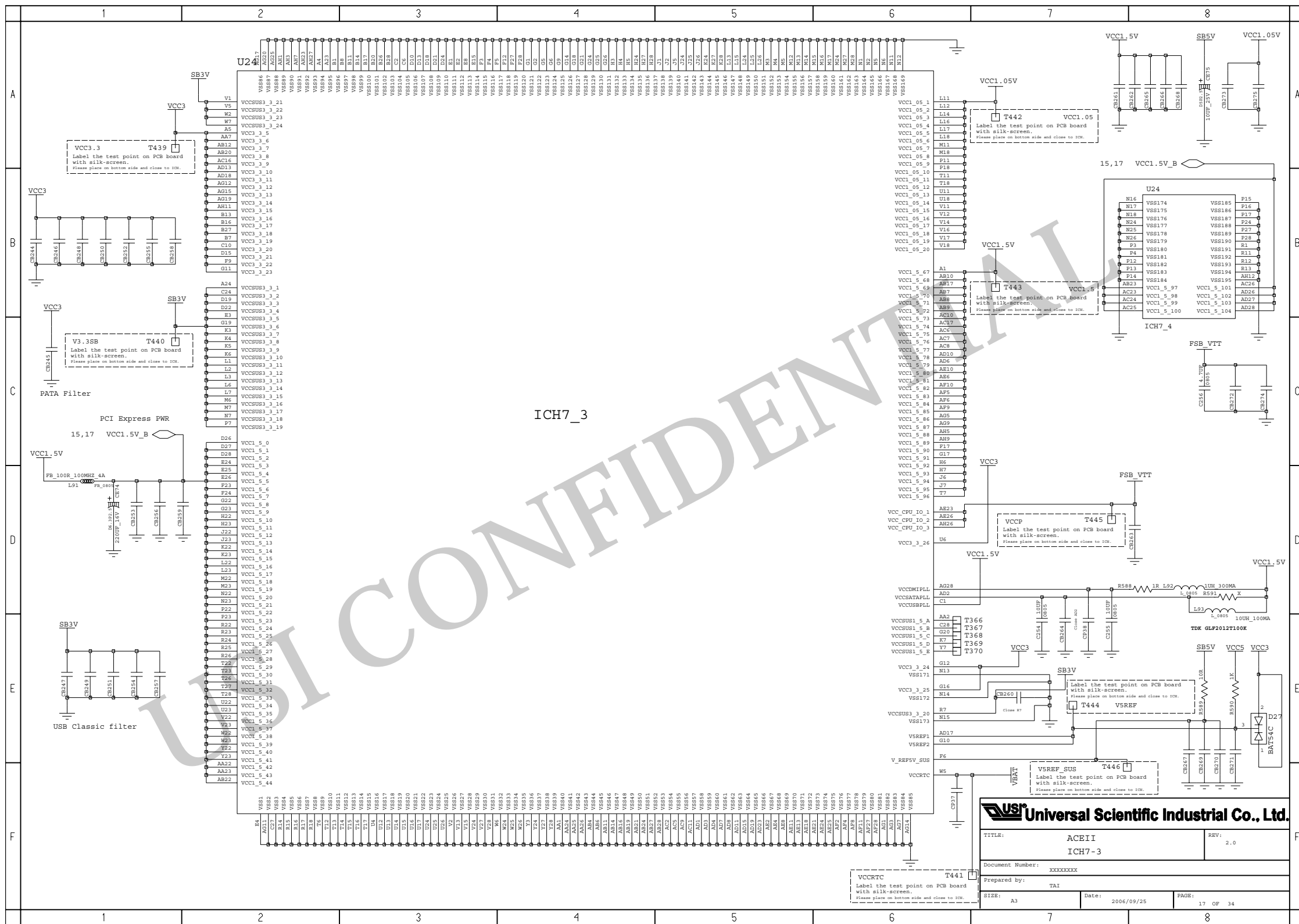
	1	2	3	4	5	6	7	8	
A	<p>Channel A VTT Decoupling Caps</p>								A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

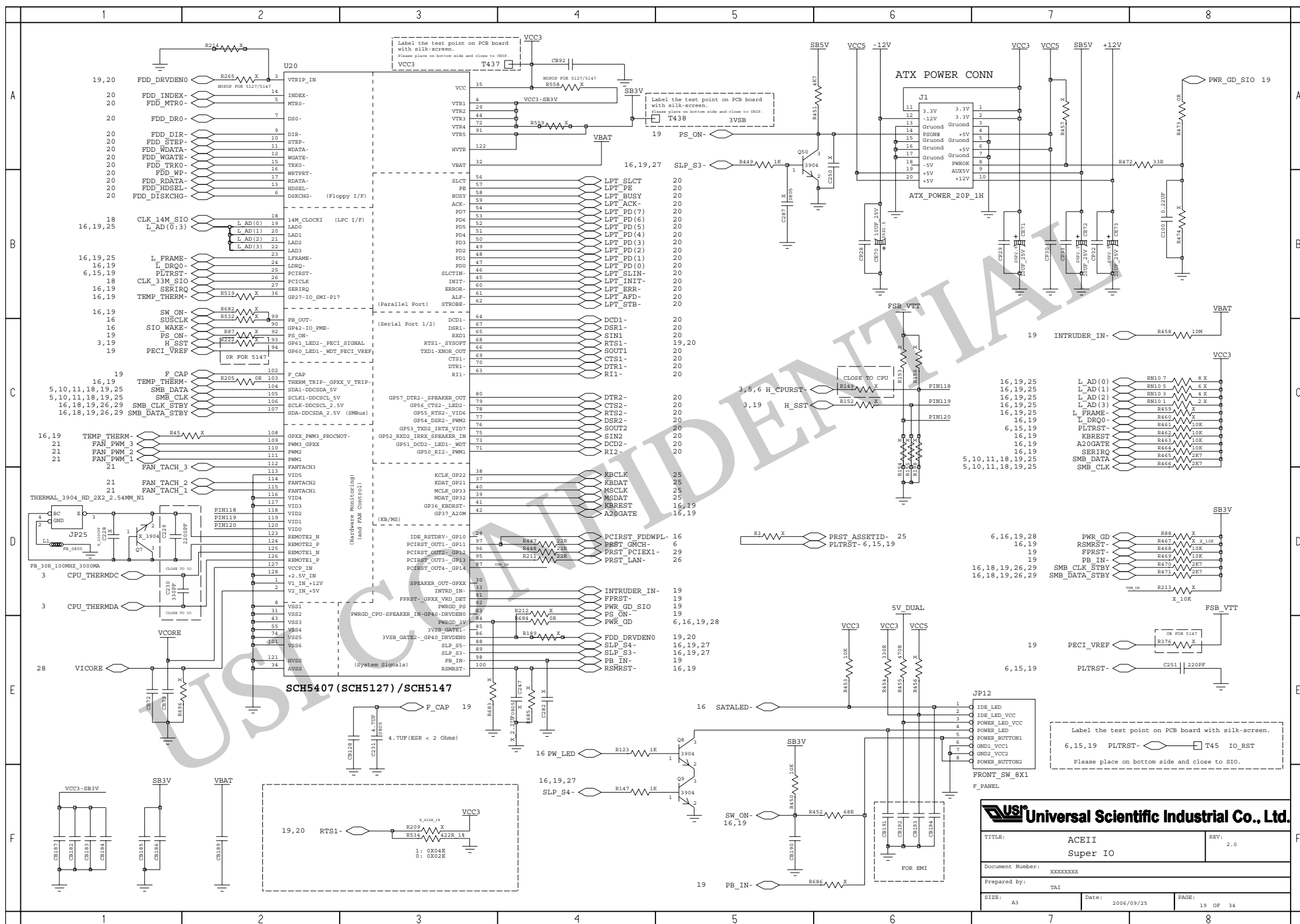


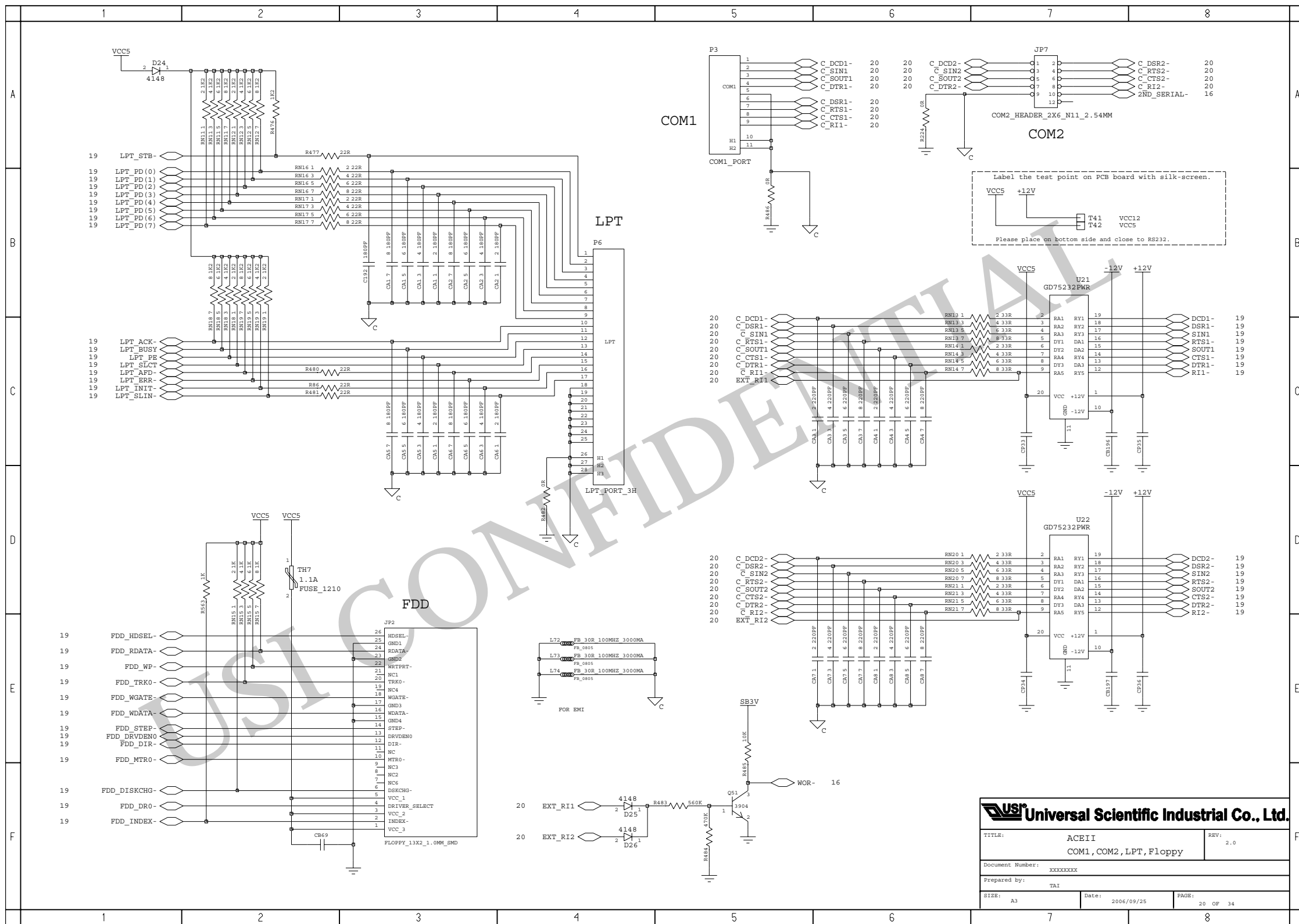


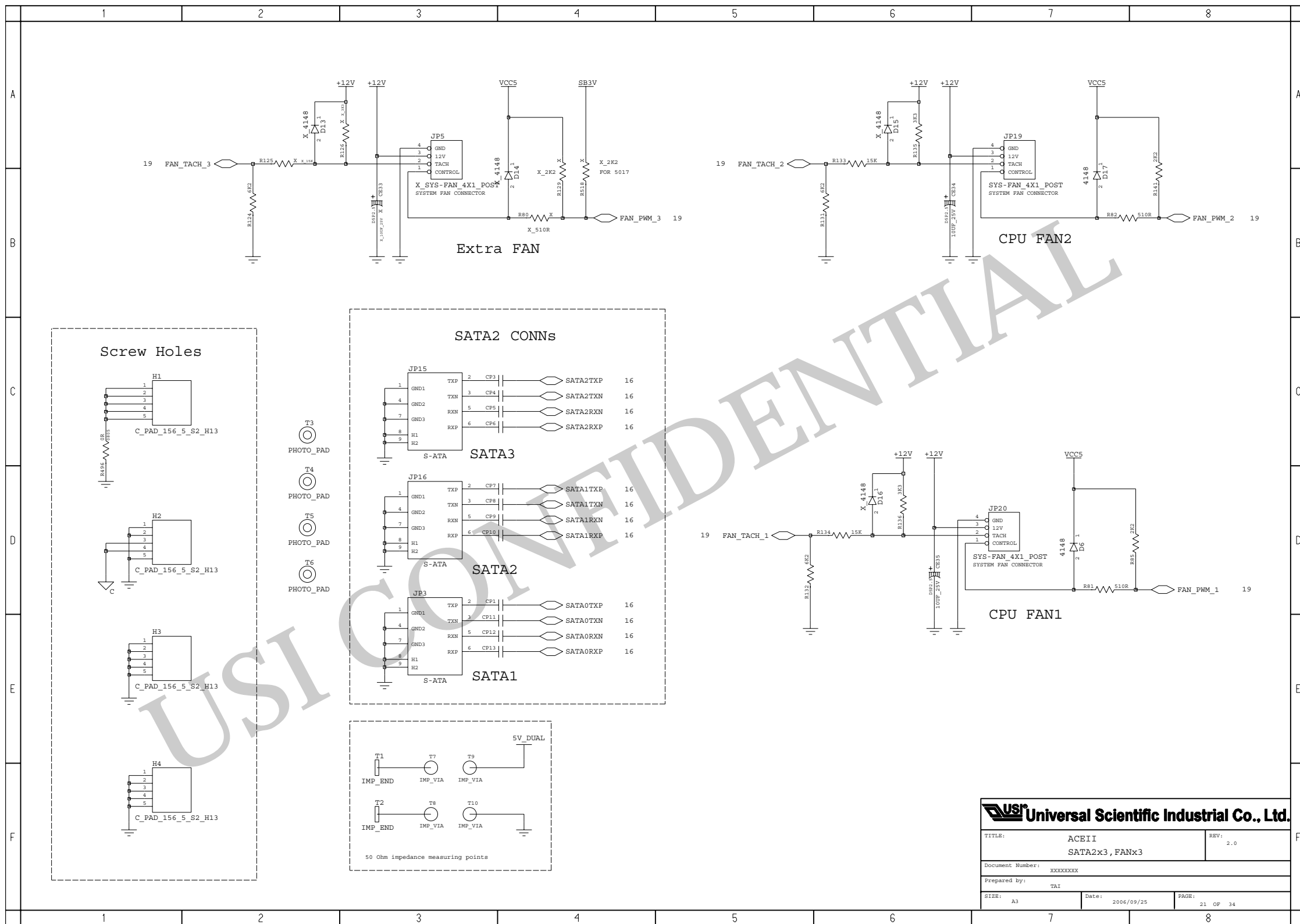






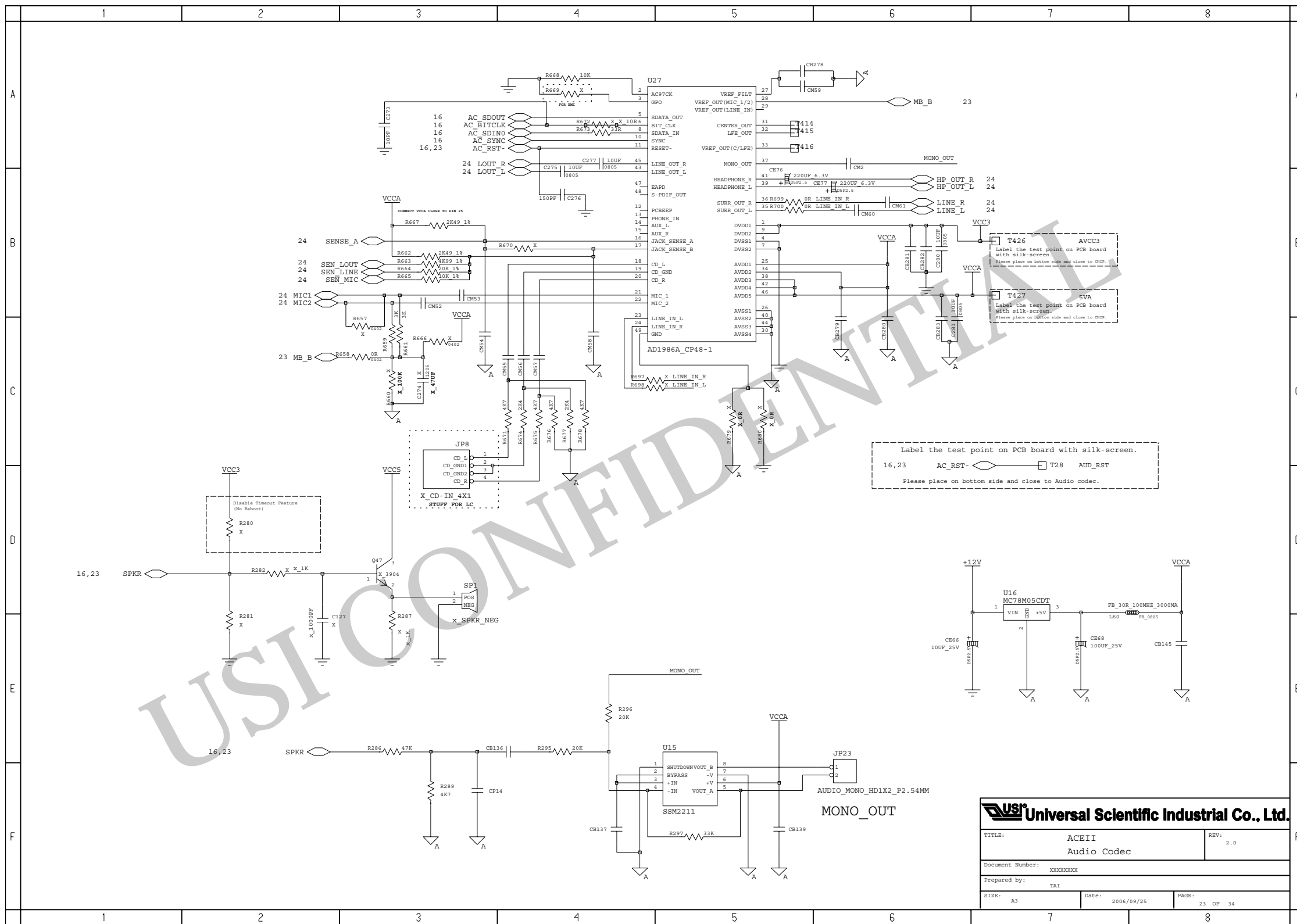


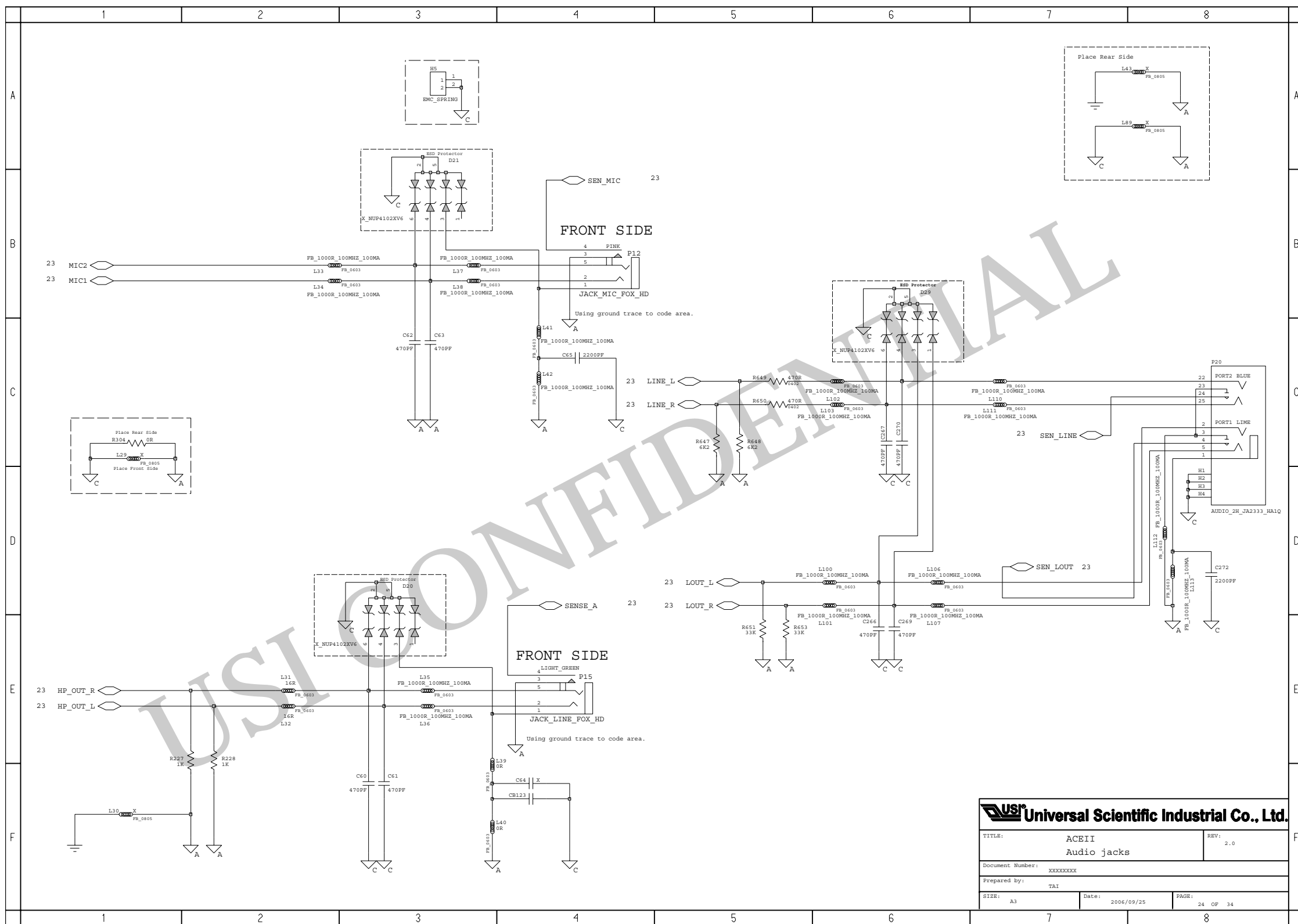




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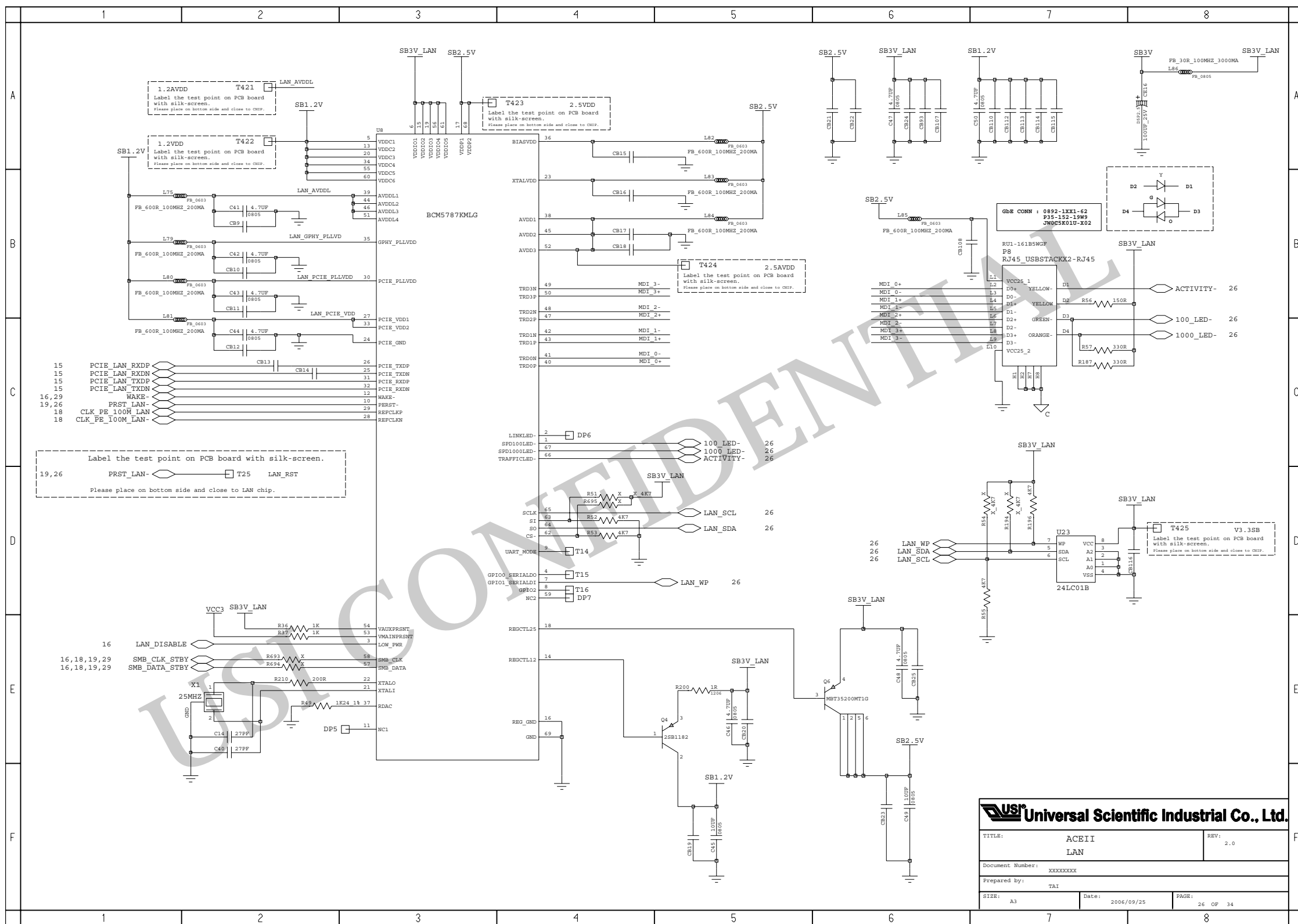
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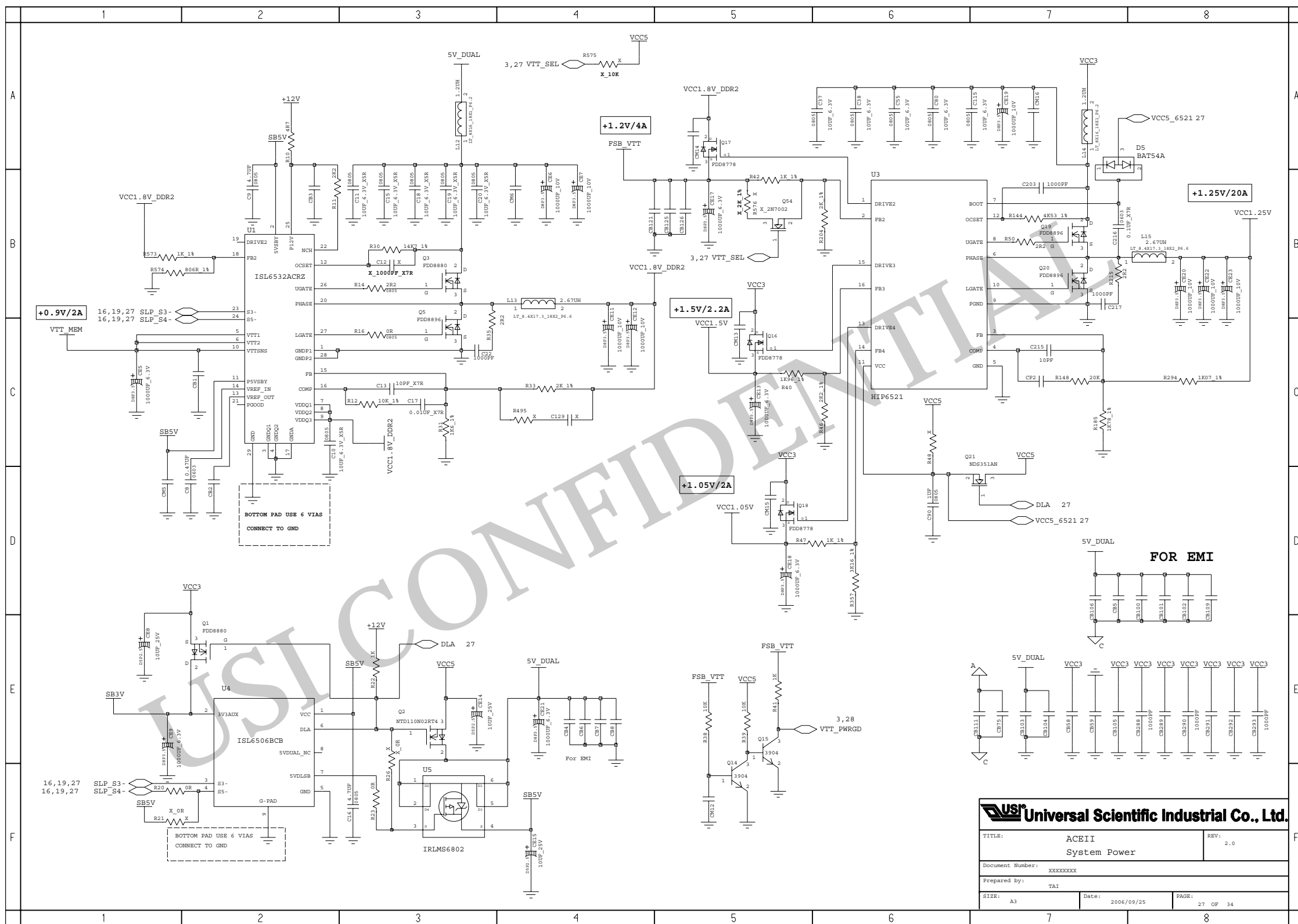


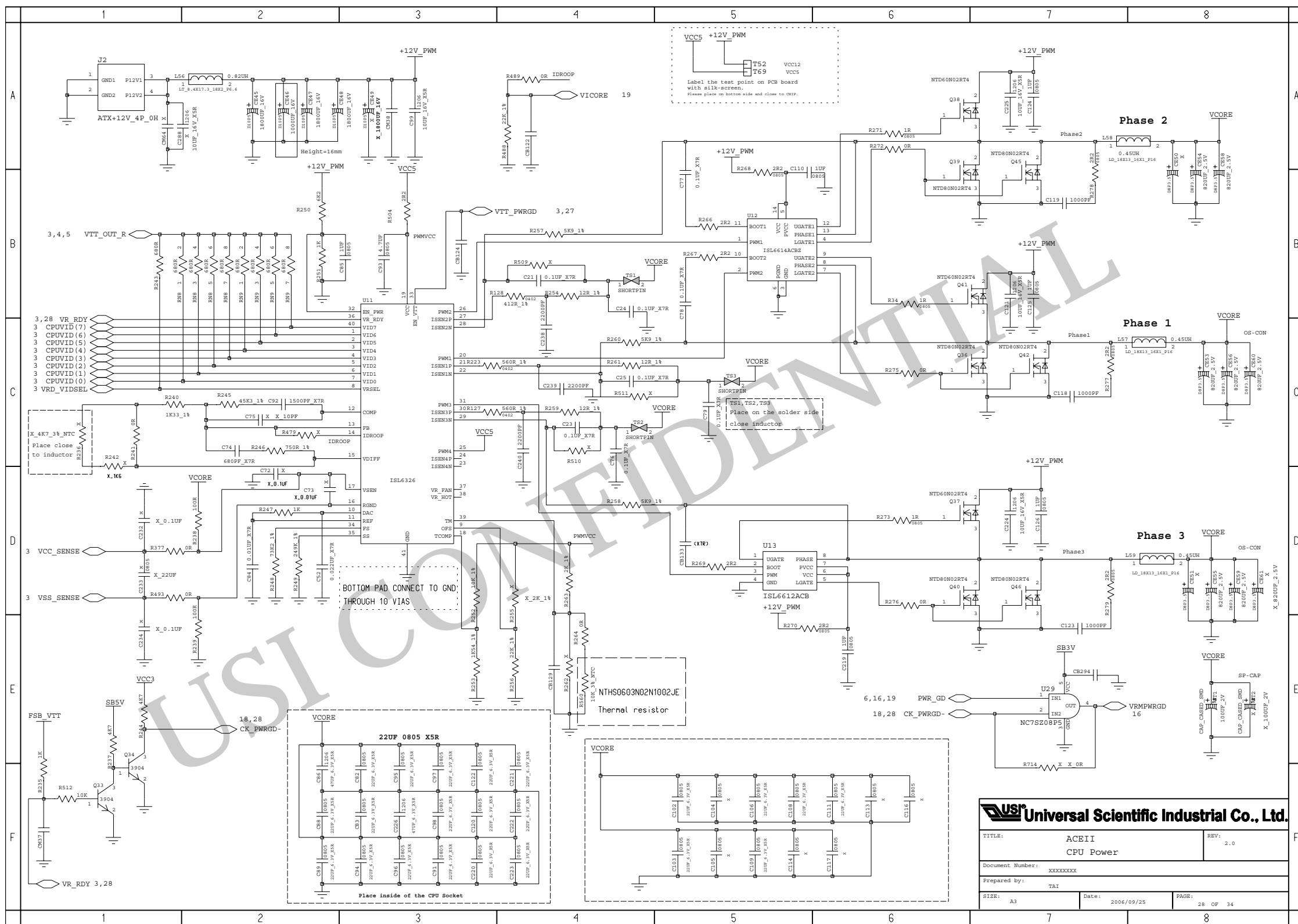


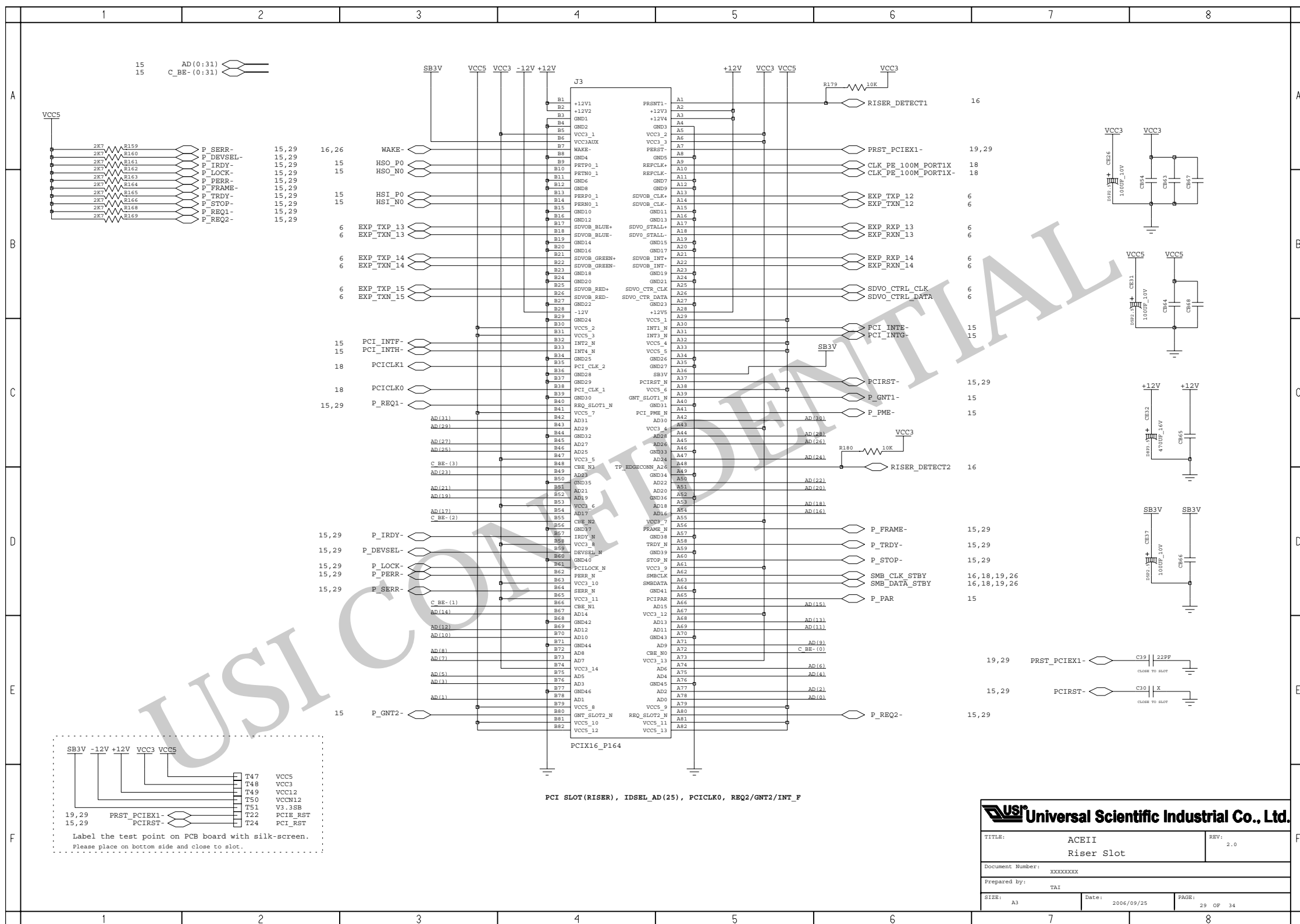
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TITLE: ACEII		REV: 2.0
Rear USBx2, KB/MS CONN		
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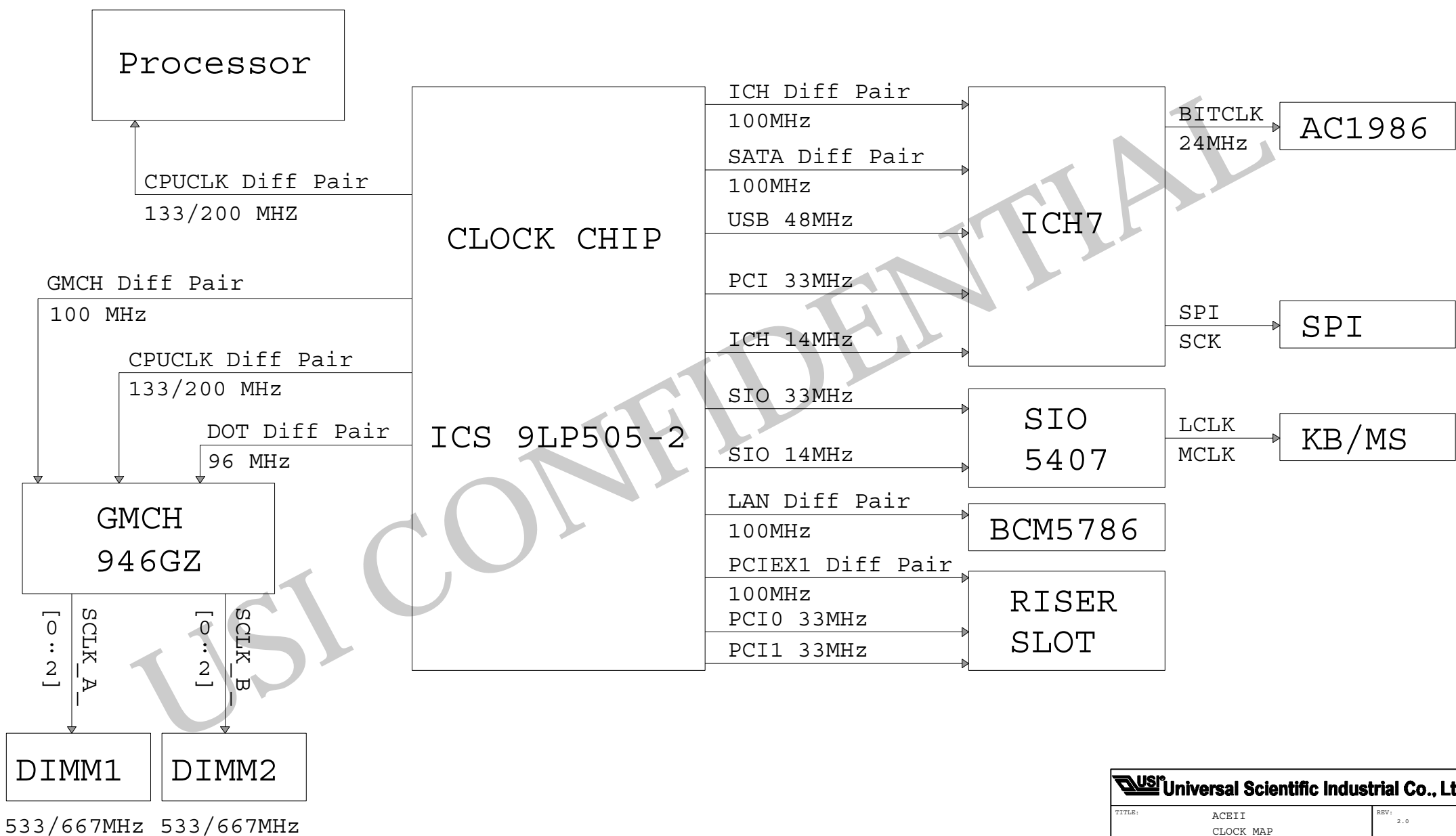




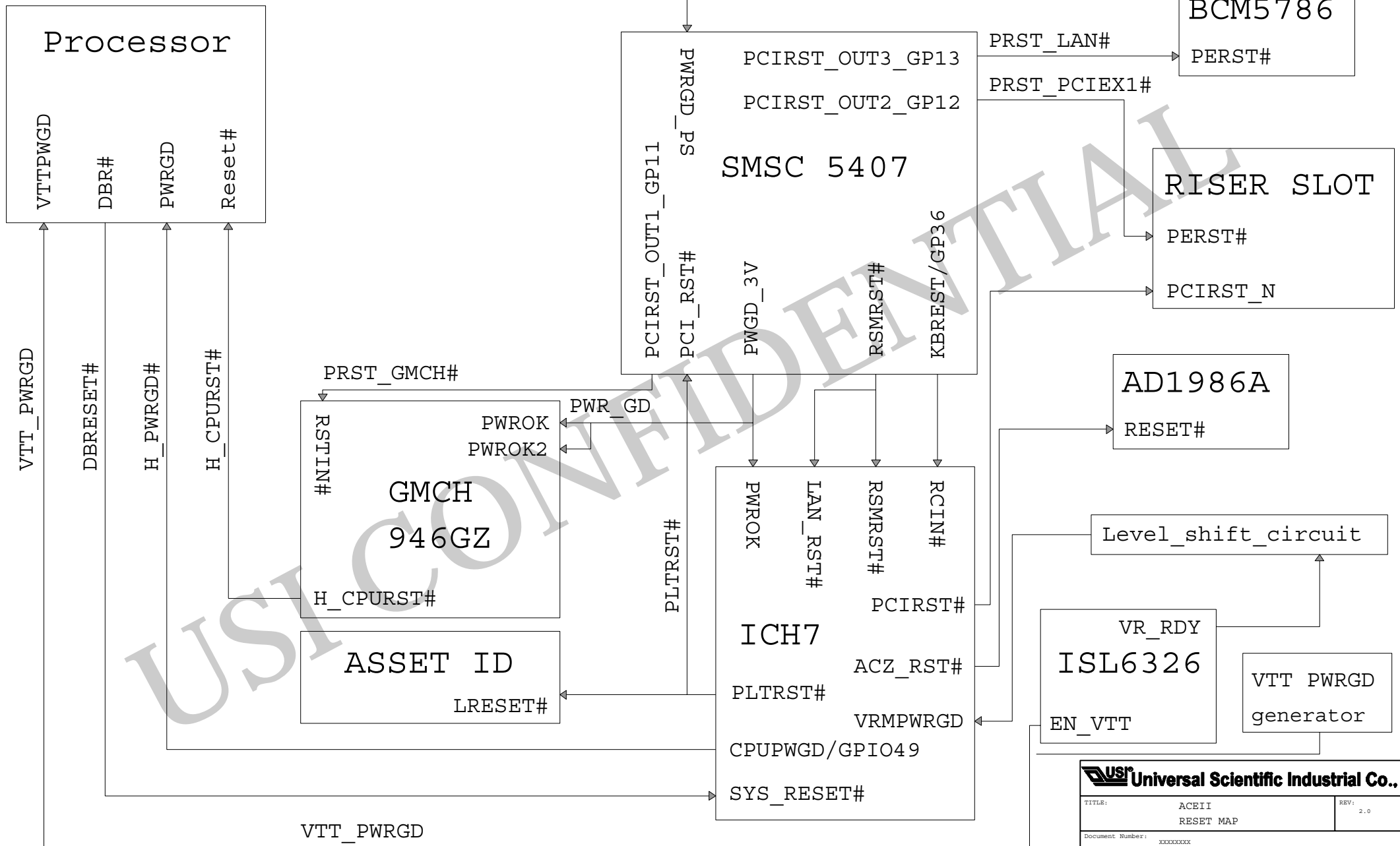




ACEII CLOCK MAP



ACEII RESET MAP



ACEII GPIO MAP

ICH7 GPIO MAP

GPIO	INPUT/OUTPUT	CHIP POWER WELL	ACEII define	Recommend
GPIO0	I/O	VCC3_3	10K Pull high	
GPIO1	I/O	VCC5	P_REQ5#	
GPIO2	I/OD	VCC3_3	PCI_INTE#	
GPIO3	I/OD	VCC3_3	PCI_INTF#	
GPIO4	I/OD	VCC3_3	PCI_INTG#	
GPIO5	I/OD	VCC3_3	PCI_INTH#	
GPIO6	I/O	VCC3_3	8.2K Pull high	
GPIO7	I/O	VCC3_3	8.2K Pull high	
GPIO8	I/O	VCC3VSB	SIO_WAKE-	
GPIO9	I/O	VCC3VSB	10K Pull high	
GPIO10	I/O	VCC3VSB	10K Pull high	
GPIO11	I/O	VCC3VSB	TEMP_THERM-	
GPIO12	I/O	VCC3VSB	10K Pull High	
GPIO13	I/O	VCC3VSB	BRD_ID0	
GPIO14	I/O	VCC3VSB	BRD_ID1	
GPIO15	I/O	VCC3VSB	BRD_ID2	
GPIO16	I/O	VCC3_3	Test Point	
GPIO17	I/O	VCC3_3	1K Pull down	
GPIO18	I/O	VCC3_3	Test Point	
GPIO19	I/O	VCC3_3	8.2K Pull High	
GPIO20	I/O	VCC3_3	Test Point	
GPIO21	I/O	VCC3_3	SPI_WP#	For flash write-protect latch
GPIO22	I/O	VCC5	P_REQ4#	
GPIO23	I/O	VCC3_3	10K Pull High	
GPIO24	I/O	VCC3VSB	LAN_DISBALE#	
GPIO25	I/O	VCC3VSB	1K Pull down	
GPIO26	I/O	VCC3VSB	POWER_LED	
GPIO27	I/O	VCC3VSB	Test Point	
GPIO28	I/O	VCC3VSB	10K Pull high	
GPIO29	I/O	VCC3VSB	OC2#	
GPIO30	I/O	VCC3VSB	OC3#	
GPIO31	I/O	VCC3VSB	OC3#	
GPIO32	I/O	VCC3_3	CLEAR_CMOS#	
GPIO33	I/O	VCC3_3	RISER_DETECT1	
GPIO34	I/O	VCC3_3	RISER_DETECT2	
GPIO35	I/O	VCC3_3	10K Pull down	
GPIO36	I/O	VCC3_3	8.2K Pull High	
GPIO37	I/O	VCC3_3	8.2K Pull High	
GPIO38	I/O	VCC3_3	2ND_SERIAL#	
GPIO39	I/O	VCC3_3	10K Pull High	
GPIO[40:47]	N/A	N/A	N/A	
GPIO48	I/O	VCC3_3	1K Pull high	
GPIO49	I/O	CPU_IO	H_PWRGD#	

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POWER ON SEQUENCE DIAGRAM

SB5V

SB3V

PWRBTN#

PSON#

SLP_S3#

SLP_S4#

VCC5 , VCC3 , +12

5V_DUAL

VCC1.8V_DDR2

VTT_MEM

VCC1.25V

VCC1.5V

VCC1.05V

FSB_VTT

VTT_PWRGD

VCORE

VRMPWRGD

PWR_GD_SIO

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POWER SEQUENCE

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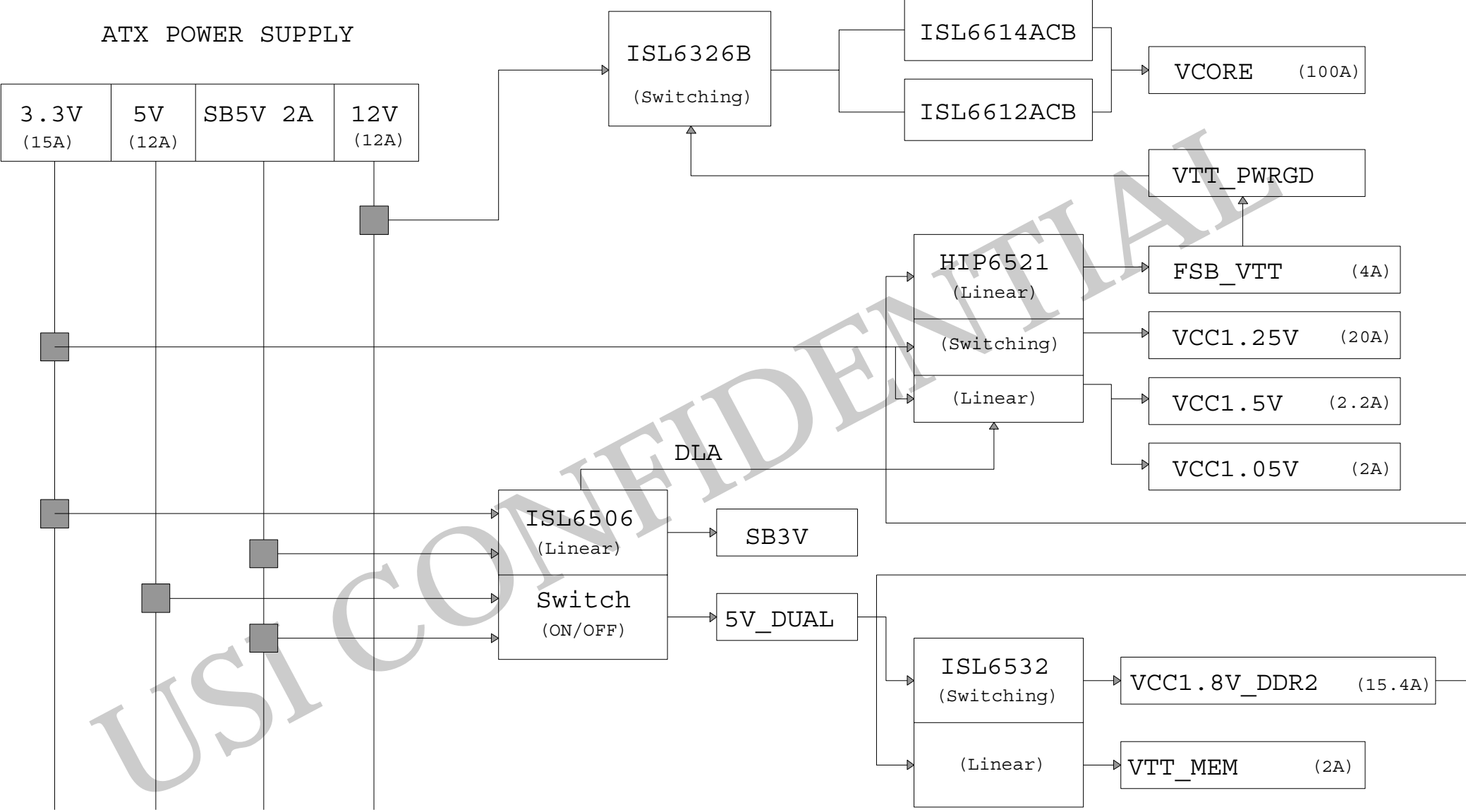
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POWER DELIVERY MAP

ATX POWER SUPPLY



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